A 1GHz 133.9fJ Neural Spike Sorting 6-bit Absolute-Value Detector

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I. BACKGROUND OF DESIGN

To solve the problem of comparing the absolute value of a 6-bit neural spike input (X) to some threshold (T), we opted for a custom design using static CMOS and PTL that effectively combines calculating the absolute value and comparison into a single logic stage. Our goal was to output 1 if |X| > T and 0 otherwise.

In order to avoid creating an adder (to add 1 after flipping bits in the case of a negative input) and then a comparator, we took advantage of the conditions on input: X will range from -31 to 31 and T is guaranteed to be positive. If we assume that we have access to the absolute value of X, then we can figure out whether |X| > T by using properties of 2's complement and bit-wise addition. By flipping all of the bits of T and adding to |X|, we can use knowledge of carries and MSBs to determine the answer. When T's bits are flipped, this represents inverting the sign and subtracting 1: $\overline{T} = -T - 1$. If we add |X| to \overline{T} , the sum will be zero or positive so long as |X| > T, since \overline{T} is one less than the negative of T. The problem has been reduced to determining whether a sum is positive or not.

By inverting T, we guarantee that the MSB of \overline{T} will be 1. Assuming |X| is available, we also know that the MSB of |X|will be 0. Therefore, the only way to make the sum positive is if the carry-out (C5) of the fifth bit is 1. In this case, |X| > Tand output is 1. If C5 is 0, then the sum will be negative and $|X| \leq T$, with output 0. Our implementation focuses on calculating a 5th bit carry out by using the same logic as a carry lookahead adder would, sans any sum logic. By using CLA logic, we also realized that we could incorporate the absolute-value generator into the carry logic and save an extra adder by setting $C_{in} = 1$ when X is negative (sixth bit is 1).

The logical expression for C5 is:

$$C_5 = G_4 + G_3 P_4 + G_2 P_4 P_3 + G_1 P_4 P_3 P_2 + G_0 P_4 P_3 P_2 P_1 + C_{in} P_4 P_3 P_2 P_1 P_0$$
(1)

In order to save transistors, this can be factored:

$$C_5 = G_4 + P_4(G_3 + P_3(G_2 + P_2(G_1 + P_1(G_0 + P_0C_{in})))) \quad (2)$$

II. IMPLEMENTATION

The input stage consists of an input buffer, a MUX to select between X or \overline{X} , and an intermediate stage output buffer. The sixth bit of X is used as the selector for the MUX. If X is negative, \overline{X} is selected as input to the second stage. Otherwise, X is passed directly to an output buffer and then to the second stage. The MSB of X is also passed into the C_{in} port of the second stage. Therefore, if X is negative, the second stage will receive the flipped bits and automatically incorporate addition by 1 via C_{in} , effectively calculating |X|. The second stage calculates C_5 .



Figure 1: Stage 1 input buffer and MUXes.

The critical path is from $\overline{X_0}$ input to the output C_5 . This

signal travels through 2 inverters and a T-gate in the first stage, and 9 NOR gates, 2 NAND gates, and 4 inverters in the second stage.

Delay was decreased by reducing the size of fan-out 1 gates to 325:325nm, 325:215nm, 325:215nm for NAND, NOR, and NOT respectively. Since the fan-out of C_5 is 32 reference inverters, we sized the output inverter by 4x to 2.6:1.72um and gradually decreased the driving capability upstream. The $(n-1)^th$ NOR gate was sized at 1.3um:860nm. The $(n-2)^th$ NOR gate was sized at 650:430nm.

III. LAYOUT

Our layout prioritized minimization of wire lengths. It ended up having an aspect ratio of 1.61. Area minimization was also prioritized, which resulted in a narrow, taller design and hence a larger than expected aspect ratio. When taking into consideration our space savings, area was $0.631um^2$. The X limit was 21.905nm and the Y limit was 35.48nm.

The layout has indentations which reduce the total area, but since aspect ratio is calculated based on the limits of X and Y, this does not improve our ratio.



Figure 2: Layout cell showing stage 1 integrated with stage 2. The critical path is also shown traced in gray. The yellow boxes outline some of the logical sub-cells.

The critical path is from X_0 input through the carry logic and to the output. This signal goes through the most gates. For reference, the carry logic path can be seen in figure 7 on the last page. It can be represented as follows:

$$t_{crit} = t_{TGate} + 2 * t_{NAND} + 4 * t_{NOT} + 9 * t_{NOR}$$
(3)

It was expected that NOR gates would contribute the most to delay on a unit-level.

IV. SIMULATION RESULTS

The circuit is functionally correct. Results of the testbench simulation are shown below, with Vdd = 1v.



Figure 3: Functional check confirming that output is as expected. This was run at Vdd = 1v.

This minimal design allowed us to scale Vdd to 587.5mV without exceeding the limit of the clock period. Energy was 133.946 fJ. The worst case $t_p = 994.267 ps$ was within the limit of the clock period (1ns) and was through the critical path. This is shown in Figure 3.

It's possible to maintain low energy usage while leaving enough headroom to compensate for any timing issues. Practically speaking, this is the case that this circuit might operate in when inserted between clocked modules. At Vdd = 612.5mV, there is approximately 106ps of headroom, with a critical path delay $t_p = 893.999ps$. This case is shown in Figure 4.

The best-case delay occurs at the worst-case energy usage point, when Vdd = 1v. Energy was 396.79fJ and critical path delay was $t_p = 370.679ps$. This is shown in figure 5.

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16 tplh_X3_OUT	229.545p	V	V	
17 tphI_X3_OUT	238.615p			
18 tplh_X4_OUT	171.748p	V		
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20 tplh_X5_OUT	177.662p			
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24 Delay_X3_OUT	234.08p		V	
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Design Varia

Figure 4: Test bench result with Vdd=587.5mV. This represents the best-case energy and worst-case delay since it approaches the 1ns limit.

Figure 6:Test bench result with Vdd=1V. This is the best-case delay and worst-case energy.

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	16 tplh_X3	_OUT		506.659p	V	V	
	17 tphl_X3	_OUT		574.755p		V	
	18 tplh_X4	_OUT		363.278p			
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	25 Delay	X2 OUT		658.12p			
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	27 Delay	X0 OUT		893.999p			
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Figure 5:Test bench result with Vdd = 612.5mV. This is a headroom case.

Carry logic shown below. Stage 1 is represented as black box in the upper left corner.



Figure 7: C_5 logic calculation. Stage 1 is shown as a black box on the upper left.