A 1GHz 133.9fJ Neural Spike Sorting 6-bit Absolute-Value Detector

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I. Background of Design

To solve the problem of comparing the absolute value of a 6-bit neural spike input (X) to some threshold (T), we opted for a custom design using static CMOS and PTL that effectively combines calculating the absolute value and comparison into a single logic stage. Our goal was to output 1 if $|X| > T$ and 0 otherwise.

In order to avoid creating an adder (to add 1 after flipping bits in the case of a negative input) and then a comparator, we took advantage of the conditions on input: X will range from -31 to 31 and T is guaranteed to be positive. If we assume that we have access to the absolute value of X, then we can figure out whether $|X| > T$ by using properties of 2's complement and bit-wise addition. By flipping all of the bits of T and adding to $|X|$, we can use knowledge of carries and MSBs to determine the answer. When T's bits are flipped, this represents inverting the sign and subtracting 1: $\overline{T} = -T - 1$. If we add $|X|$ to $\overline{T}$, the sum will be zero or positive so long as $|X| > T$, since $\overline{T}$ is one less than the negative of T. The problem has been reduced to determining whether a sum is positive or not.

By inverting T, we guarantee that the MSB of $\overline{T}$ will be 1. Assuming $|X|$ is available, we also know that the MSB of $|X|$ will be 0. Therefore, the only way to make the sum positive is if the carry-out (C5) of the fifth bit is 1. In this case, $|X| > T$ and output is 1. If C5 is 0, then the sum will be negative and $|X| \leq T$, with output 0. Our implementation focuses on calculating a 5th bit carry out by using the same logic as a carry lookahead adder would, sans any sum logic. By using CLA logic, we also realized that we could incorporate the absolute-value generator into the carry logic and save an extra adder by setting $C_{in} = 1$ when X is negative (sixth bit is 1).

The logical expression for C5 is:

$$\begin{aligned} C_5 = G_4 + G_3P_4 + G_2P_4P_3 + G_1P_4P_3P_2 \\ +G_0P_4P_3P_2P_1 + C_{in}P_4P_3P_2P_1P_0 \end{aligned} \quad (1)$$

In order to save transistors, this can be factored:

$$C_5 = G_4+P_4(G_3+P_3(G_2+P_2(G_1+P_1(G_0+P_0C_{in})))) \quad (2)$$

II. Implementation

The input stage consists of an input buffer, a MUX to select between X or $\overline{X}$, and an intermediate stage output buffer. The sixth bit of X is used as the selector for the MUX. If X is negative, $\overline{X}$ is selected as input to the second stage. Otherwise, X is passed directly to an output buffer and then to the second stage. The MSB of X is also passed into the C_{in} port of the second stage. Therefore, if X is negative, the second stage will receive the flipped bits and automatically incorporate addition by 1 via C_{in}, effectively calculating $|X|$. The second stage calculates C_5.

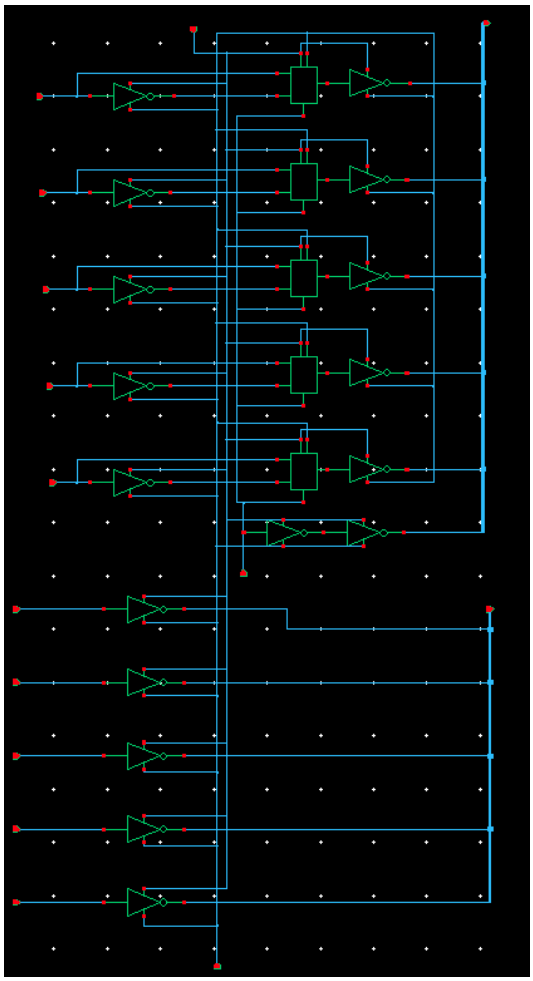

Figure 1: Stage 1 input buffer and MUXes.

The critical path is from $\overline{X_0}$ input to the output C_5. This

signal travels through 2 inverters and a T-gate in the first stage, and 9 NOR gates, 2 NAND gates, and 4 inverters in the second stage.

Delay was decreased by reducing the size of fan-out 1 gates to 325:325nm, 325:215nm, 325:215nm for NAND, NOR, and NOT respectively. Since the fan-out of C_5 is 32 reference inverters, we sized the output inverter by 4x to 2.6:1.72um and gradually decreased the driving capability upstream. The $(n-1)^th$ NOR gate was sized at 1.3um:860nm. The $(n-2)^th$ NOR gate was sized at 650:430nm.

III. Layout

Our layout prioritized minimization of wire lengths. It ended up having an aspect ratio of 1.61. Area minimization was also prioritized, which resulted in a narrow, taller design and hence a larger than expected aspect ratio. When taking into consideration our space savings, area was $0.631um^2$. The X limit was 21.905nm and the Y limit was 35.48nm.

The layout has indentations which reduce the total area, but since aspect ratio is calculated based on the limits of X and Y, this does not improve our ratio.

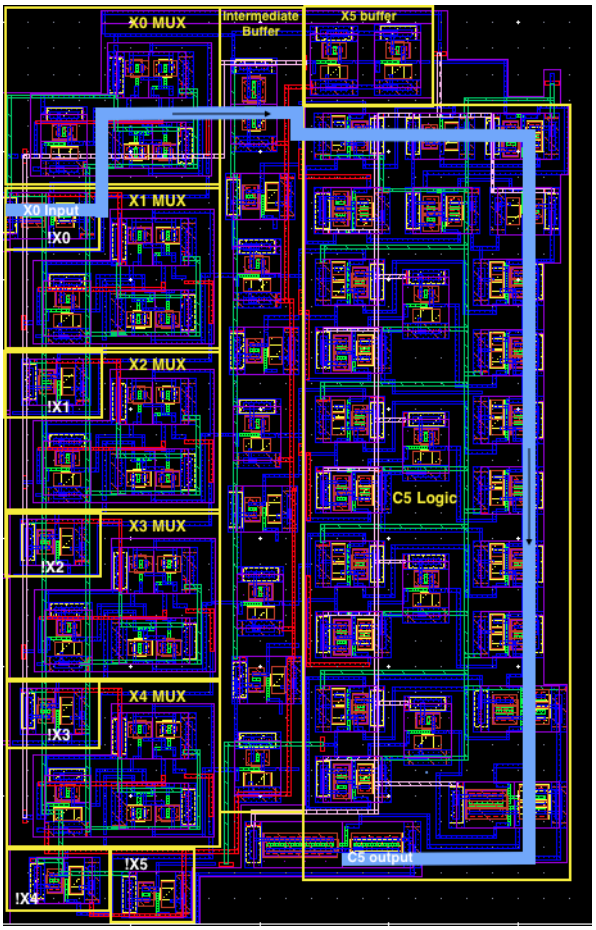

Figure 2: Layout cell showing stage 1 integrated with stage 2. The critical path is also shown traced in gray. The yellow boxes outline some of the logical sub-cells.

The critical path is from X_0 input through the carry logic and to the output. This signal goes through the most gates. For reference, the carry logic path can be seen in figure 7 on the last page. It can be represented as follows:

$$t_{crit} = t_{TGate} + 2 * t_{NAND} + 4 * t_{NOT} + 9 * t_{NOR} \quad (3)$$

It was expected that NOR gates would contribute the most to delay on a unit-level.

IV. Simulation Results

The circuit is functionally correct. Results of the testbench simulation are shown below, with $Vdd = 1v$.

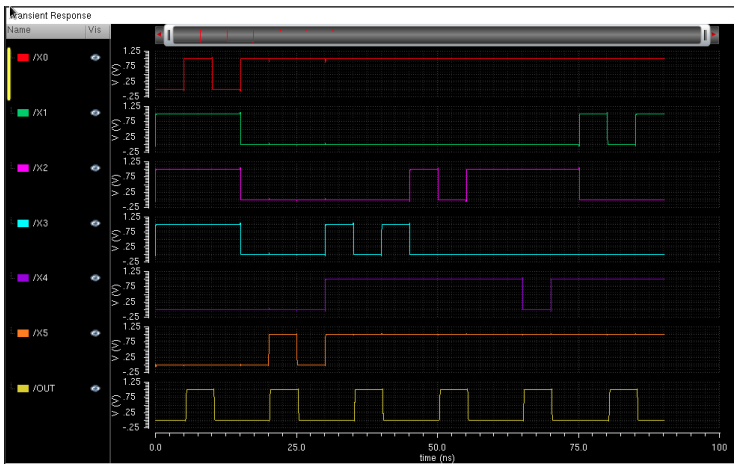

Figure 3: Functional check confirming that output is as expected. This was run at $Vdd = 1v$.

This minimal design allowed us to scale Vdd to $587.5mV$ without exceeding the limit of the clock period. Energy was $133.946fJ$. The worst case $t_p = 994.267ps$ was within the limit of the clock period (1ns) and was through the critical path. This is shown in Figure 3.

It's possible to maintain low energy usage while leaving enough headroom to compensate for any timing issues. Practically speaking, this is the case that this circuit might operate in when inserted between clocked modules. At $Vdd = 612.5mV$, there is approximately 106ps of headroom, with a critical path delay $t_p = 893.999ps$. This case is shown in Figure 4.

The best-case delay occurs at the worst-case energy usage point, when $Vdd = 1v$. Energy was $396.79fJ$ and critical path delay was $t_p = 370.679ps$. This is shown in figure 5.

Design Variables

	Name	Value
1	VDD	587.5m
2	VEXT	1

Analyses

	Type	Enable	Arguments
1	tran	☑	0 90.1n moderate
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	X0		☑	☑	allv
2	X1		☑	☐	allv
3	X2		☑	☐	allv
4	X3		☑	☑	allv
5	X4		☑	☐	allv
6	X5		☑	☑	allv
7	OUT		☑	☑	allv
8	V0/MINUS		☐	☑	yes
9	V0/PLUS		☐	☑	yes
10	tplh_X0_OUT	956.694p	☐	☑	
11	tphl_X0_OUT	1.03164n	☐	☑	
12	tplh_X1_OUT	820.848p	☑	☐	
13	tphl_X1_OUT	898.184p	☑	☐	
14	tplh_X2_OUT	689.103p	☑	☑	
15	tphl_X2_OUT	767.414p	☑	☑	
16	tplh_X3_OUT	559.081p	☑	☑	
17	tphl_X3_OUT	636.611p	☑	☑	
18	tplh_X4_OUT	399.268p	☑	☐	
19	tphl_X4_OUT	408.368p	☑	☐	
20	tplh_X5_OUT	416.635p	☑	☑	
21	tphl_X5_OUT	735.101p	☑	☑	
22	Delay_X5_OUT	575.868p	☑	☑	
23	Delay_X4_OUT	403.818p	☑	☐	
24	Delay_X3_OUT	597.846p	☑	☑	
25	Delay_X2_OUT	728.258p	☑	☑	
26	Delay_X1_OUT	859.516p	☑	☐	
27	Delay_X0_OUT	994.267p	☑	☑	
28	Energy	133.946f	☑	☑	

Figure 4: Test bench result with $Vdd = 587.5mV$. This represents the best-case energy and worst-case delay since it approaches the 1ns limit.

Design Variables

	Name	Value
1	VDD	612.5m
2	VEXT	1

Analyses

	Type	Enable	Arguments
1	tran	☑	0 90.1n moderate
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	X0		☑	☑	allv
2	X1		☑	☐	allv
3	X2		☑	☐	allv
4	X3		☑	☑	allv
5	X4		☑	☐	allv
6	X5		☑	☑	allv
7	OUT		☑	☑	allv
8	V0/MINUS		☐	☑	yes
9	V0/PLUS		☐	☑	yes
10	tplh_X0_OUT	860.302p	☐	☑	
11	tphl_X0_OUT	927.696p	☐	☑	
12	tplh_X1_OUT	742.179p	☑	☐	
13	tphl_X1_OUT	810.098p	☑	☐	
14	tplh_X2_OUT	623.813p	☑	☑	
15	tphl_X2_OUT	692.428p	☑	☑	
16	tplh_X3_OUT	506.659p	☑	☑	
17	tphl_X3_OUT	574.755p	☑	☑	
18	tplh_X4_OUT	363.278p	☑	☐	
19	tphl_X4_OUT	371.351p	☑	☐	
20	tplh_X5_OUT	380.279p	☑	☑	
21	tphl_X5_OUT	660.233p	☑	☑	
22	Delay_X5_OUT	520.256p	☑	☑	
23	Delay_X4_OUT	367.314p	☑	☐	
24	Delay_X3_OUT	540.707p	☑	☑	
25	Delay_X2_OUT	658.12p	☑	☑	
26	Delay_X1_OUT	776.139p	☑	☐	
27	Delay_X0_OUT	893.999p	☑	☑	
28	Energy	145.414f	☑	☑	

Figure 5:Test bench result with $Vdd = 612.5mV$. This is a headroom case.

Design Variables

	Name	Value
1	VDD	1
2	VEXT	1

Analyses

	Type	Enable	Arguments
1	tran	☑	0 90.1n moderate
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	X0		☑	☑	allv
2	X1		☑	☐	allv
3	X2		☑	☐	allv
4	X3		☑	☑	allv
5	X4		☑	☐	allv
6	X5		☑	☑	allv
7	OUT		☑	☑	allv
8	V0/MINUS		☐	☑	yes
9	V0/PLUS		☐	☑	yes
10	tplh_X0_OUT	372.928p	☐	☑	
11	tphl_X0_OUT	368.429p	☐	☑	
12	tplh_X1_OUT	326.149p	☑	☐	
13	tphl_X1_OUT	335.413p	☑	☐	
14	tplh_X2_OUT	277.825p	☑	☑	
15	tphl_X2_OUT	287.004p	☑	☑	
16	tplh_X3_OUT	229.545p	☑	☑	
17	tphl_X3_OUT	238.615p	☑	☑	
18	tplh_X4_OUT	171.748p	☑	☐	
19	tphl_X4_OUT	164.051p	☑	☐	
20	tplh_X5_OUT	177.662p	☑	☑	
21	tphl_X5_OUT	259.418p	☑	☑	
22	Delay_X5_OUT	218.54p	☑	☑	
23	Delay_X4_OUT	167.899p	☑	☐	
24	Delay_X3_OUT	234.08p	☑	☑	
25	Delay_X2_OUT	282.414p	☑	☑	
26	Delay_X1_OUT	330.781p	☑	☐	
27	Delay_X0_OUT	370.679p	☑	☑	
28	Energy	396.79f	☑	☑	

Figure 6:Test bench result with $Vdd = 1V$. This is the best-case delay and worst-case energy.

Carry logic shown below. Stage 1 is represented as black box in the upper left corner.

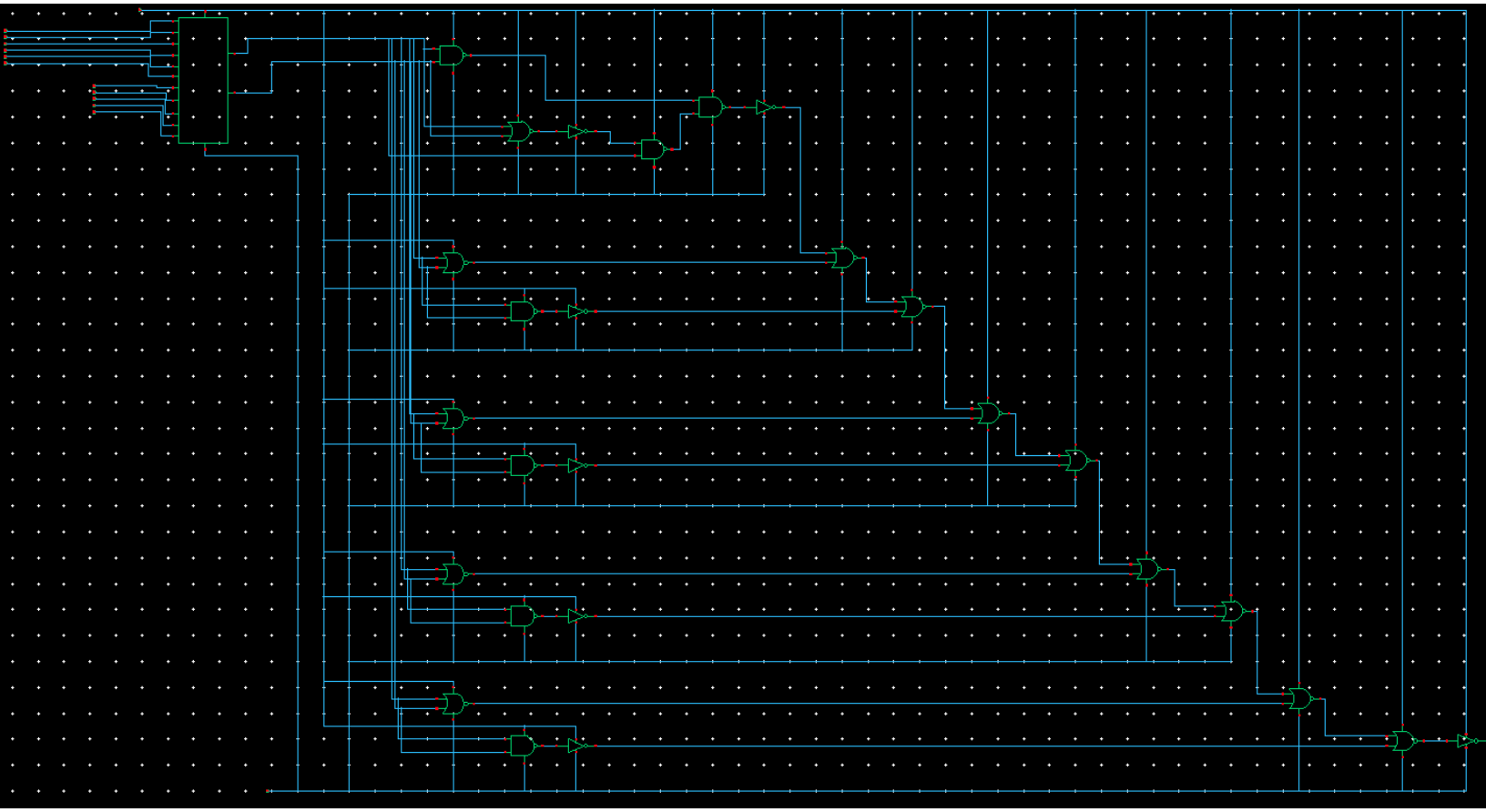

Figure 7: C_5 **logic calculation. Stage 1 is shown as a black box on the upper left.**